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ABSTRACT OF THE DISCLOSURE

A method and system for clock synchronization of semiconductor devices. The method uses a master-slave configuration to designate a semiconductor device with the lowest rate clock source as a master device and zero all clock sources inside the semiconductor device in order to output the zeroing lowest rate clock source to slave devices for clock synchronization of all clock sources respectively in the slave devices, and further implements a phase checker in each semiconductor device to ensure clock synchronization inside and between the semiconductor devices, so required clock signals are precisely provided to next internal circuits of the semiconductor devices.